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Physical Implementation of CMOS Chips

Jan Ludvik

ASICentrum Brno

April 2024

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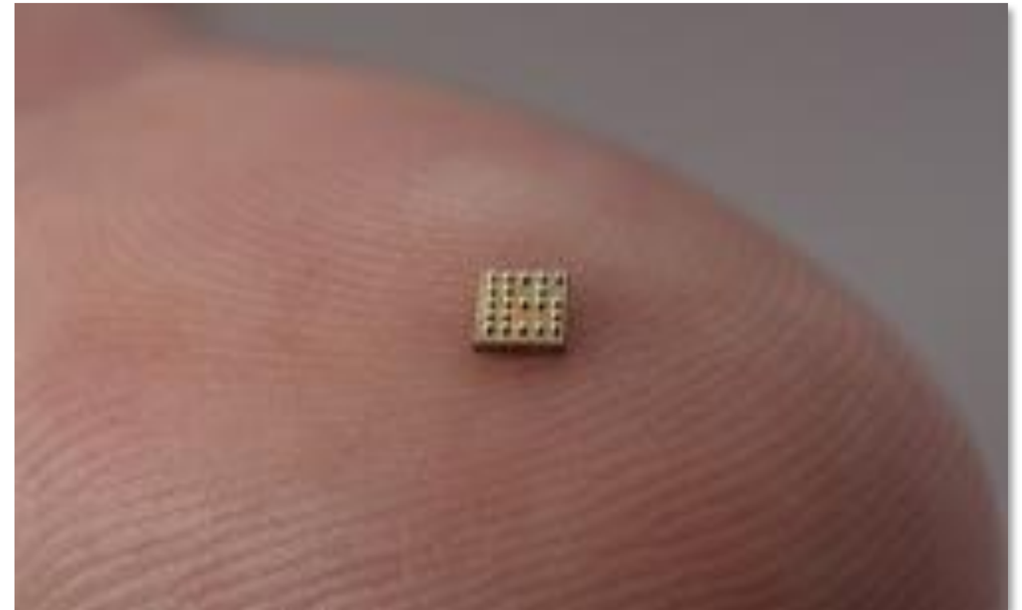
What Can You Expect? See a Teaser below.

- See a process of a digital chip (DoT) development from RTL to a packaged chip
- How digital code is compiled into a gate netlist
- DFT starts in the beginning of the flow
- Place gates, create clock trees and route nets
- Everything is optimized
- Everything is verified, at least twice
- Prepare data for manufacturing
- Each chip in a nice package
- Test, test and test



About Me.

- **Jan Ludvik** – a physical design engineer
  - **UMEL** FEKT VUT Brno
  - **Phillips Semiconductors** – Standard cells development
  - **NXP** – Standard cells development and verification
  - **onsemi** – Test vehicle physical development and verification
  - **ASICentrum** – Digital design physical development and verification

    - jan.ludvik@asicentrum.com, +420 704 972 518
    - www.asicentrum.com
    - Purkyňova 648/125, Brno 61200, Czechia

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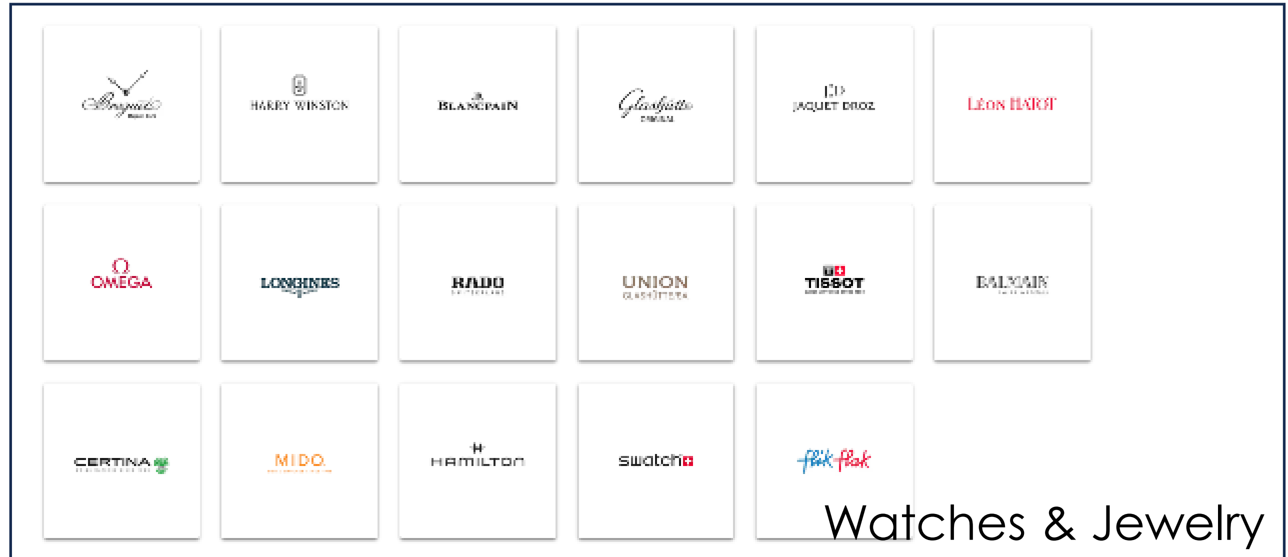
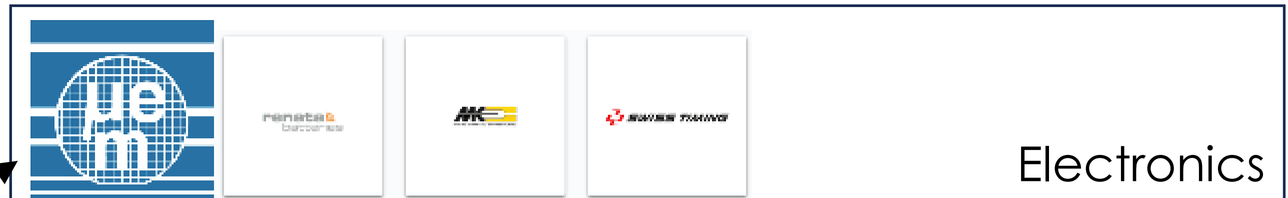
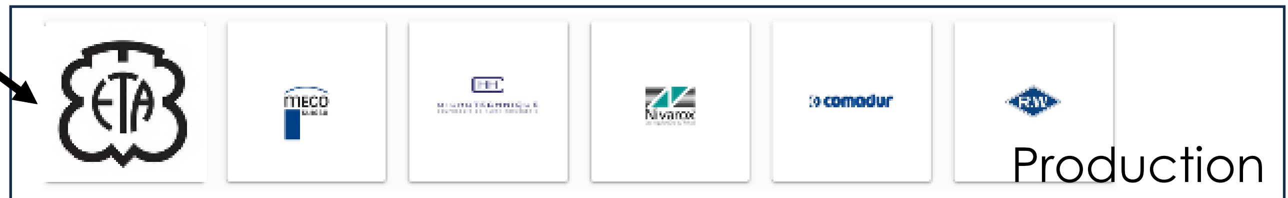


Watches & Jewelry



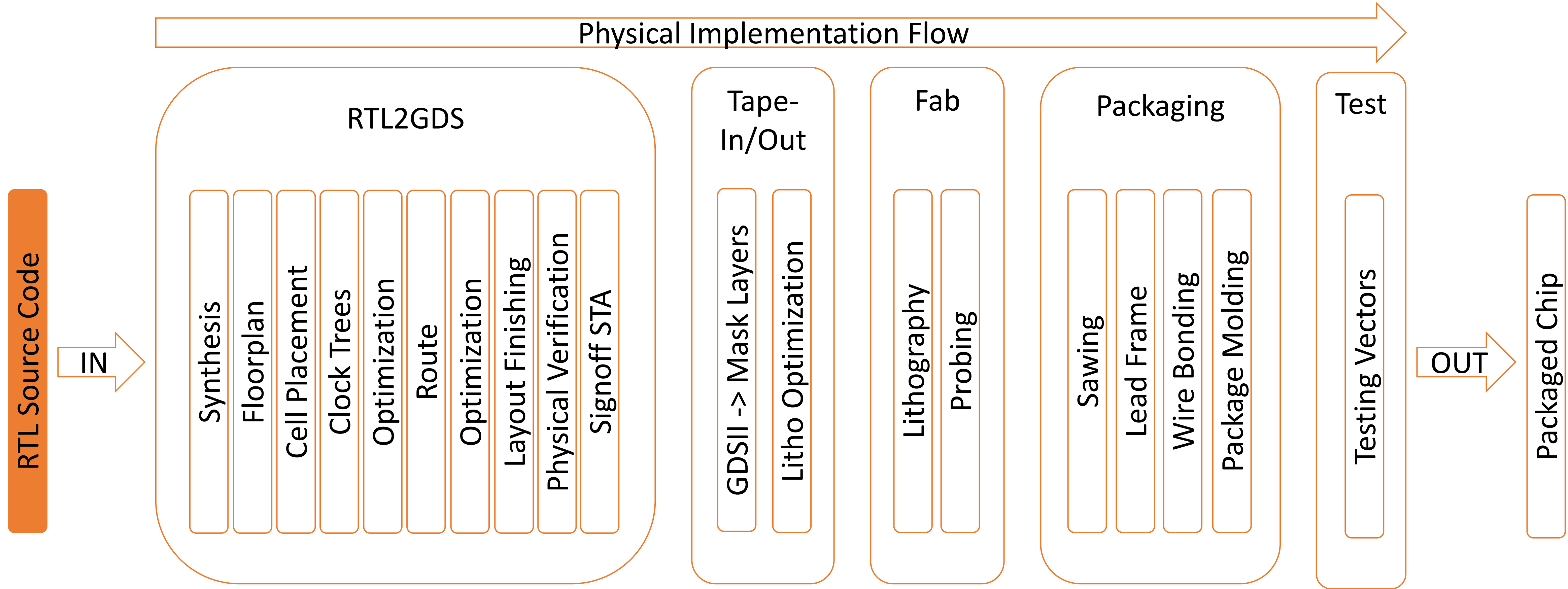
Electronics



Production

Swatch Group

Path from Inputs to Outputs



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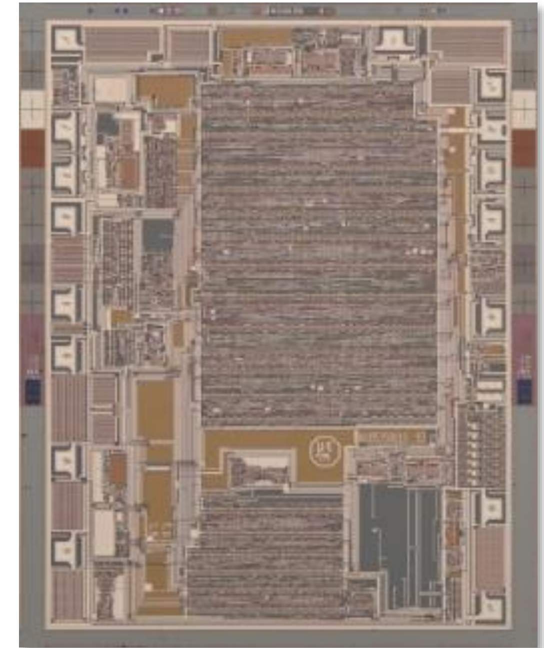
RTL2GDS

Make a physical design from a code

You Have Digital Code, so What’s next?

- What is your application?
  - Digital simulation/verification
    - Use your computer
  - Prototyping or low volume production
    - Go **FPGA**
      - Relatively low fixed costs
      - Relatively high price per a unit
  - Mass production
    - **ASIC** is the only way
      - Relatively high fixed costs (development, manufacturing, packaging)
      - Low price per a chip



RTL2GDS – Physical Design

- Inputs
  - RTL code (Verilog, SV, VHDL)
  - Technology
- Main Steps
  - **Synthesis**
  - **Place and route**
  - **Verification**
- Outputs
  - GDSII layout file
  - Tons of reports and logs

Prepare Your Working Tools

cadence

- **Genus** – Synthesis, including physical synthesis and DFT
- **Innovus** – Place and route tool
- **Tempus** – Signoff STA
- **Voltus** – EMIR analysis
- **Joules** – Power analysis
- **Quantus** – Parasitic Extraction
- **Flowkit** – a tool framework for synthesis, PnR, STA and EMIR

SYNOPSYS®

- **DC/DCNXT** – Synthesis, including physical synthesis and DFT
- **ICC/ICC2** – Place and route tool
- **Fusion Compiler** – Synthesis + PnR
- **PrimeTime** – Signoff STA
- **RedHawk** – EMIR analysis
- **PrimePower** – Power analysis
- **StarRC** – Parasitic Extraction

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- **Calibre** – DRC/LVS check
- **Tessent** – DFT
- **Questa** - Verification

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Setup Comes First!

- **Setup** = Collect all data before you start.
  - **Never underestimate it**, you cannot work without a correct setup.
- What you need to start a design:
  - Die or block area
  - IO ring
  - Technology node, process, metal stack
  - Physical Development Kit (PDK)
  - Stdcells and IO cells libraries + Macro (RAM, EEPROM, PLL) digital views
    - Liberty files, LEF, Netlists, GDSII layout
  - Other data, e.g. clock trees, SDC files, UPF, physical constraints

Now Comes the Synthesis.

- **Synthesis converts digital description (RTL) into a gate level netlist (Verilog)**
- Synthesis can also add Design For Testing (DFT)
  - Scan chains, NAND chains, *BIST
- Steps:
  - **Analyze** – reads inputs (Verilog, VHDL, SV)
  - **Elaborate** - Converts a code into virtual gates
    - First setup analyses with ideal cells and ideal clocks
  - (**DFT**) – Adds DFT modules
  - **Compile** – Converts virtual gates into real cells
    - Setup analyses with real cells timing and ideal clocks
  - **Optimize** – Optimizes netlist for timing/power/leakage/area/…
- Output – Netlist + scan chains description

```
--*****************************************************************
--
-- ENTITY DECLARATION
--
--*****************************************************************

ENTITY comb IS
  GENERIC ( N : integer := 4 );
  PORT (
   clk     : in  std_logic ;
   reset   : in  std_logic ;
   input   : in  std_logic_vector (N-1 downto 0) ;
   output  : out std_logic_vector (N-1 DOWNTO 0) ;
   ci      : in  std_logic ;
   co      : out std_logic
        );
END comb ;

--*****************************************************************
--
-- BEHAVIORAL ARCHITECTURE BODY
--
--*****************************************************************

ARCHITECTURE rtl OF comb IS

SIGNAL sum          : std_logic_vector(N DOWNTO 0);
SIGNAL previous_in  : std_logic_vector(N-1 DOWNTO 0);


BEGIN

output <= sum (N-1 downto 0);
co     <= sum (N);

scitacka:
PROCESS (input, previous_in, ci)
BEGIN
       sum <= ('0' & input) + ('0' & NOT(previous_in)) + ('0' & ci)
END PROCESS scitacka;
--
accum_register:
PROCESS ( clk, reset)
BEGIN
       IF ( reset = '1') THEN    previous_in <= (OTHERS => '0');
       ELSIF (clk'EVENT AND clk'LAST_VALUE = '0' AND clk = '1' )
                         THEN    previous_in <= input;
       END IF ;
END PROCESS accum_register;
```

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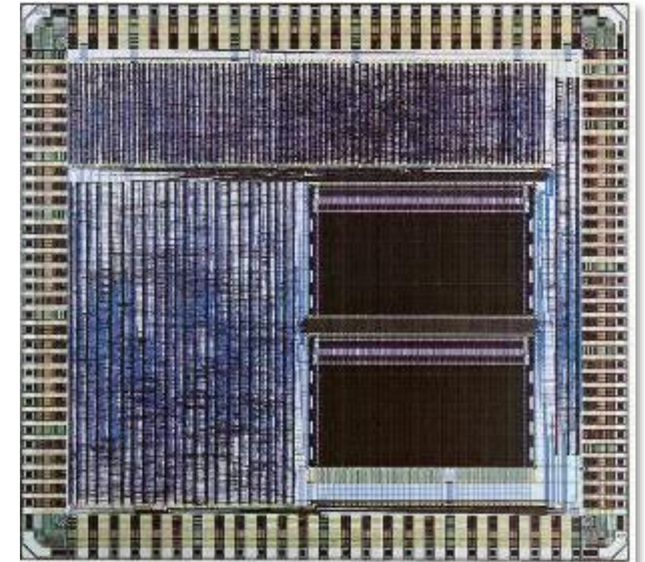
Design For Testability (DFT), Part One - Insertion

- DFT increases the certainty of your product's reliability, efficiency, and commercial success.
- RTL code based
  - It is already present in RTL
- Injected during synthesis
  - By the synthesis tool
  - By third party tool

Place and Route. Time for a Layout.

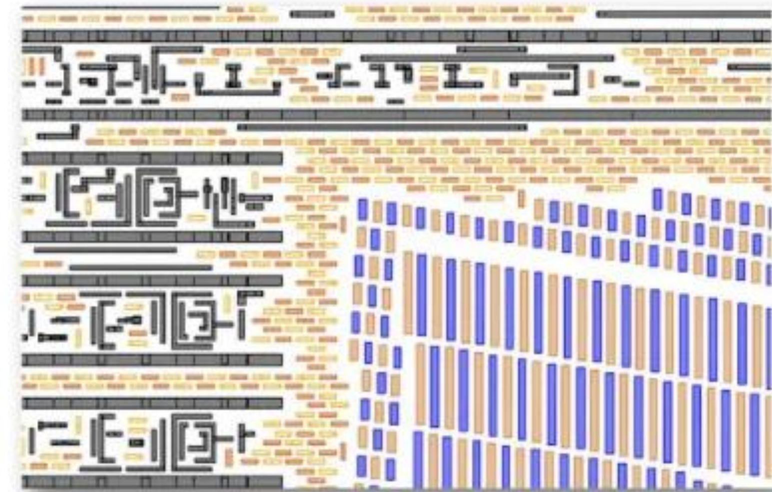
- Converts a gate level Verilog into a layout
- Steps:
  - **Floorplan**
  - Cell **placement** including optimization (S)
  - **Clock tree** generation
  - Post-clock **optimization**
  - **Routing**
  - Post-route **optimization**
  - Checks and reports (Signoff)
    - Connectivity (LVS), DRC, antenna, timing, power, …
- Output: **GDSII layout file** + reports



Finish the Layout to Create a Chip.

- Add instances or shapes which cannot be added in PnR
  - PCI test structures
  - Deep isolations (N-Buried, Deep N-Well, …)
  - Seal ring structures
  - ID label shapes

- Generate density (metal) fills
- Export the final layout
- Extract the final SPEFs



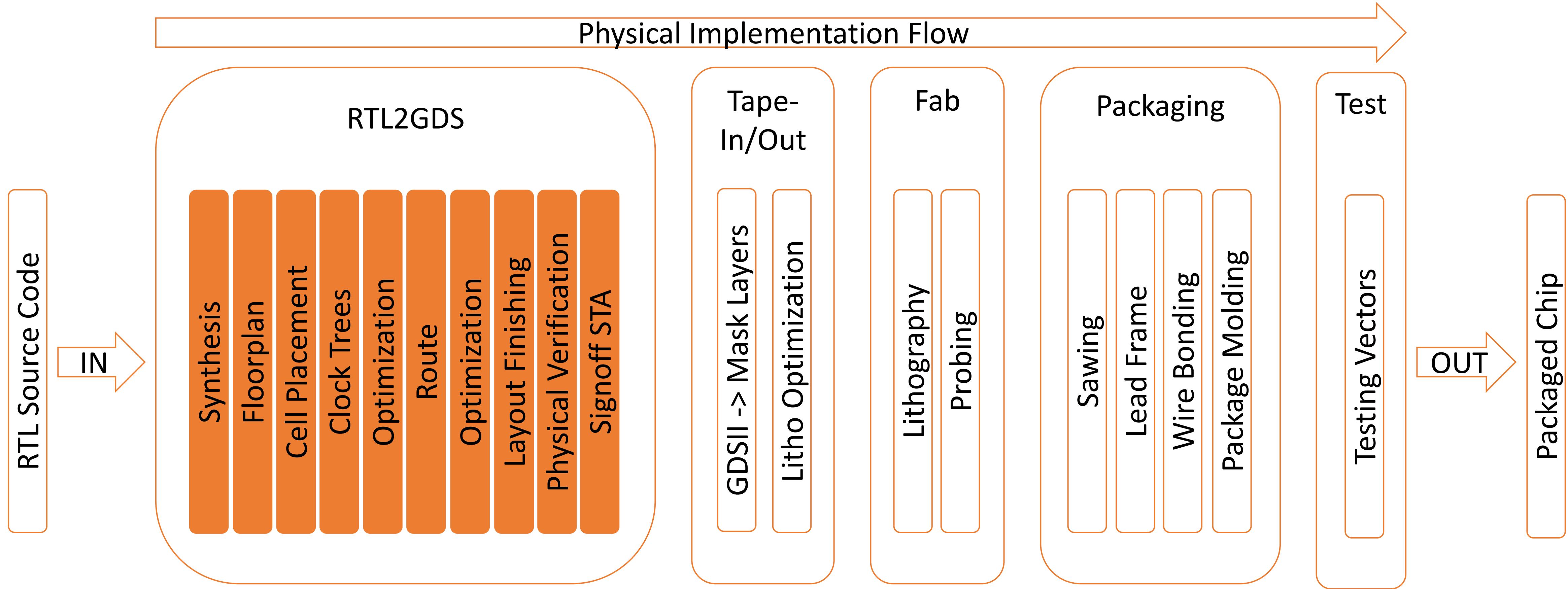
DRC and LVS, the Most Basic Physical Checks.

- Physical verification is an essential part of a design flow.
- DRC – Compare the layout to physical rules defined in the rule manual.
  - Check spacing, min/max width, distance, area, …
- LVS – Compare the design Verilog with the layout extracted netlist.
  - Check instances, pins, nets, ports and connectivity
- Other checks
  - Antenna – process antenna check
  - DFM – Additional, not required, DRC rules

Signoff STA. Design is Full of Clocks.

- **STA** – Static Timing Analysis (Simply check your timing)
  - Every signal is related to some clock.
- Run **Setup** and **Hold** analyses for ALL relevant corners and modes
- Use a final layout data, if possible
- Use signoff extracted netlists (SPEF)
- Create a back annotation (SDF)

Path from Inputs to Outputs

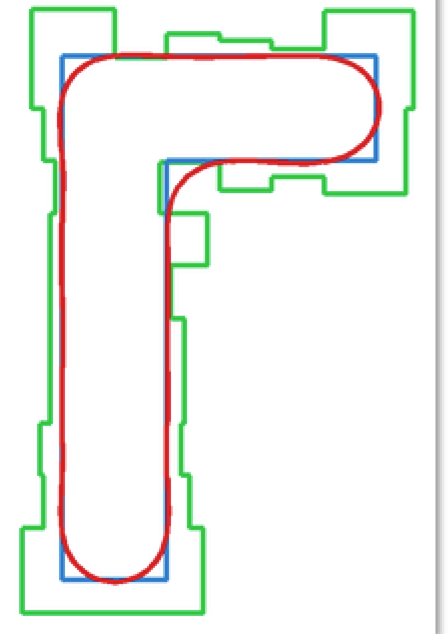


Tape-in/tape-out

Make lithographic masks from the physical design

GDSII is Good, but not Good for Masks.

- **Tape-in** is when the GDSII layout file is sent to start the process of designing lithographical masks.
  - Logical layers must be combined (AND, OR, EXOR, …).
  - Text labels are used to identify layers and deleted.
  - Optical proximity correction (**OPC**)
    - Do lithographical optimizations
  - A mask layout file is exported (usually OASIS format).
    - GDSII layers are converted into mask layers.



Your Design Is Not the Only One in the Reticle.

- A reticle is a substrate (**glass**) for the photomasks.
- Production designs are usually the only designs in the mask. **One reticle = one mask layer**.
  - Reticle size is defined by the fab.
  - Design motive (layout) is placed in the reticle many times as a matrix.
    - It is called a "**die**".
- Test designs are placed into the shuttle (MPW)
  - Combine many different designs into one die.
- **Multi Layer – Multi Die** reticle
  - Combine different designs and different layers into one reticle.

Run to the OASIS.

- Tape-in process can be done externally, it requires deep technology knowledge
- **Tape-out** in when the OASIS mask file is sent to create lithographic masks.

- Note: People usually say just “tape-out” instead of tape-in due to historical reasons.

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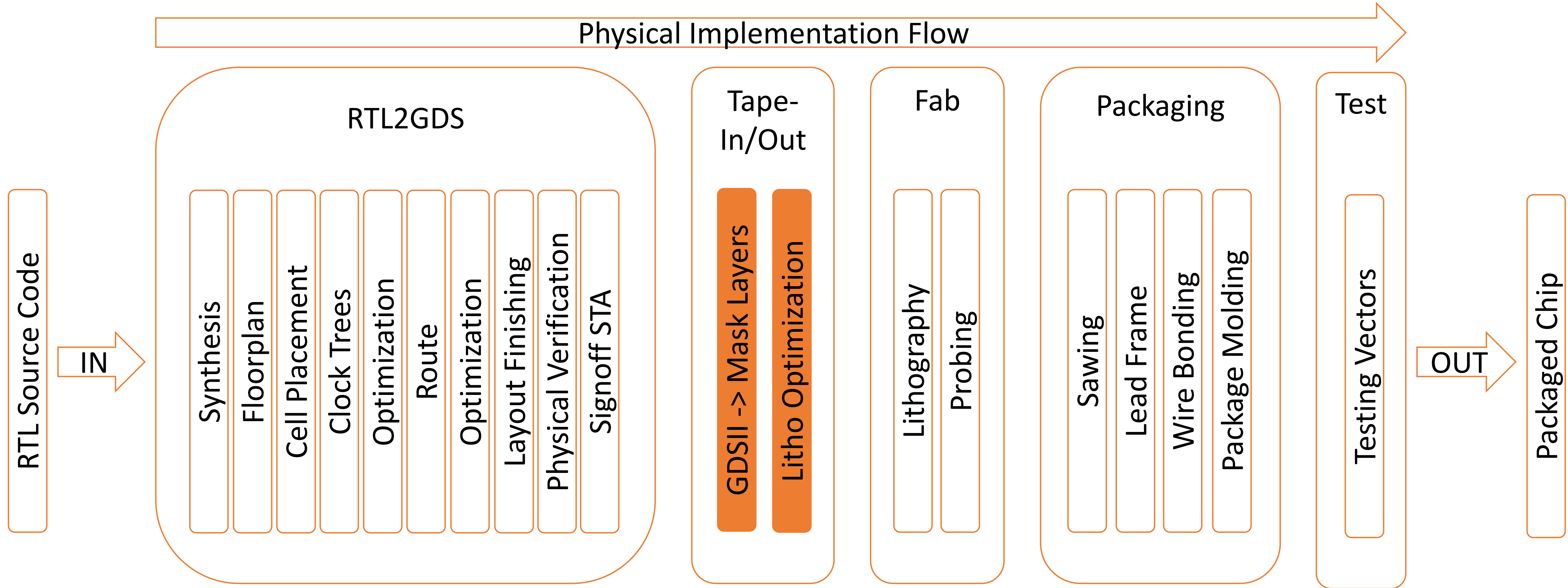
Path from Inputs to Outputs



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Semiconductor Fabrication Plant (Fab)

Make silicon wafers

Lithography, the Most Difficult Thing on Earth

- CMOS chips are made by a process called a photolithography
  - Masks are used to create a motive in all layers
  - Modern mask are very expensive due to their resolution
    - A mask set for 180 nm costs ~40k USD, 40 nm 900k USD, 3 nm many millions
- **Time** of the whole process depends on number of process **steps** and the **depth of implantation**
  - Wafer can be done in a couple of weeks or months
- Motive is “printed” step by step
  - Other process steps are common for the whole wafer

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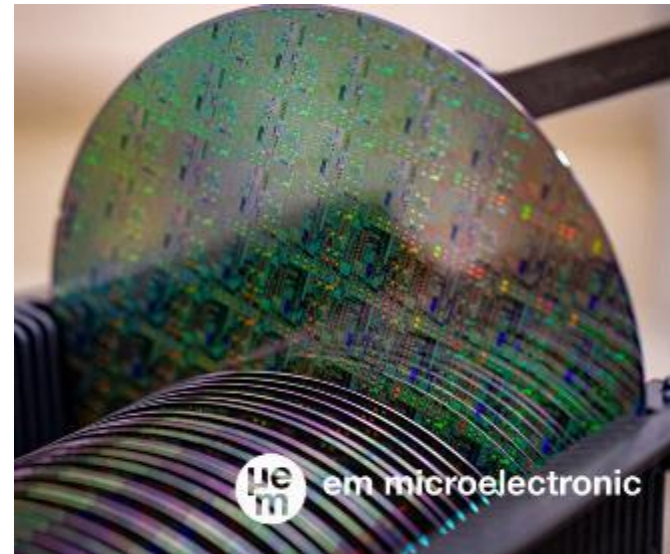
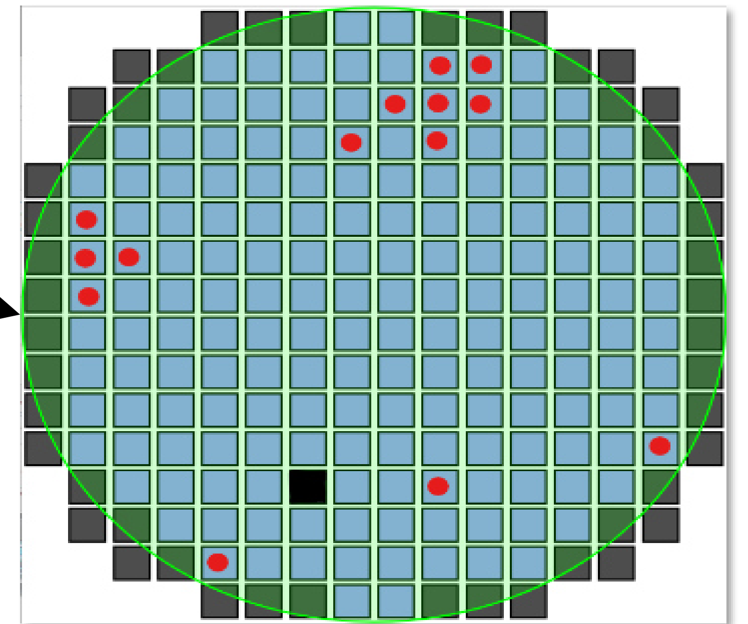
A Wafer? Standard or With Some Flavor?

- “**Lot**” is a set of silicon wafers (~25 pieces) running through the fab together in one dose.
- **Production** chips are done in a “**target process**” – process fully characterized for the mass production
- **Test vehicles** can be run also in some shifted processes
  - They are called “**flavors**”
  - Fast, slow, fast-N, slow-P, …



Don’t Be Lost, Use Your Wafer Map!

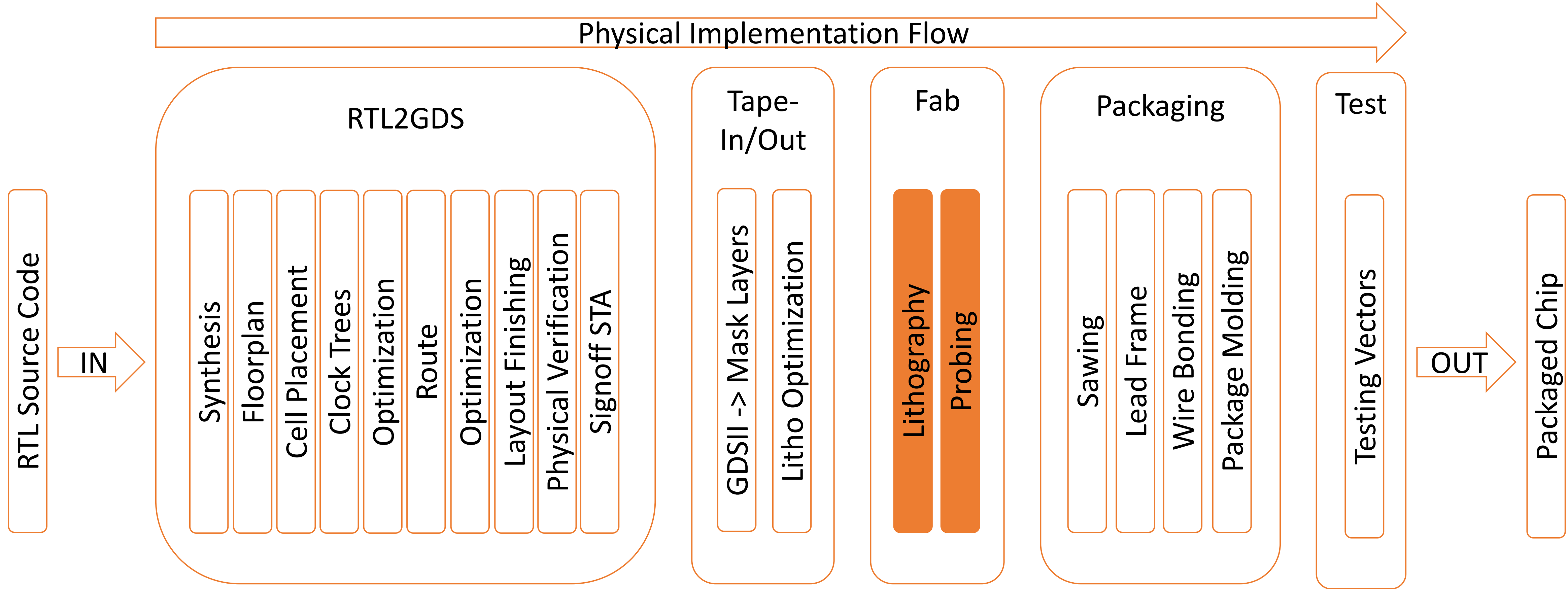
- The reticle is used in the wafer repetitively in a matrix.
- Some dies are partially out of the wafer.
- Some dies have different properties dependent on the **position** on the wafer.
- We need a **wafer map** for our orientation.



When You Have the Needles.

- **Probe** the wafer using a probe card to see if the chip lives.
  - Read a chip identifier or run some tests.
- Running **tests** before packaging can save some time and money.
  - ATE (Automatic test equipment) – standard tests
  - Custom test – BISTs, ESD, frequency, logic response, …
- **Program** OTP, flash or eePROMs.
  - Load a code or create a unique chip ID.

Path from Inputs to Outputs



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Packaging

Make “the Chip”

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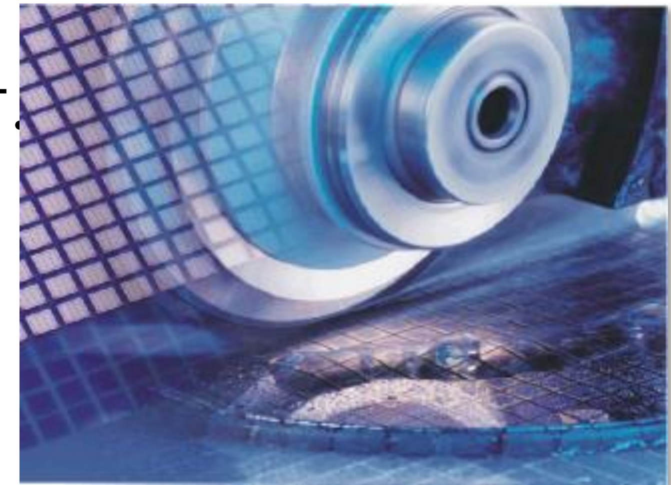
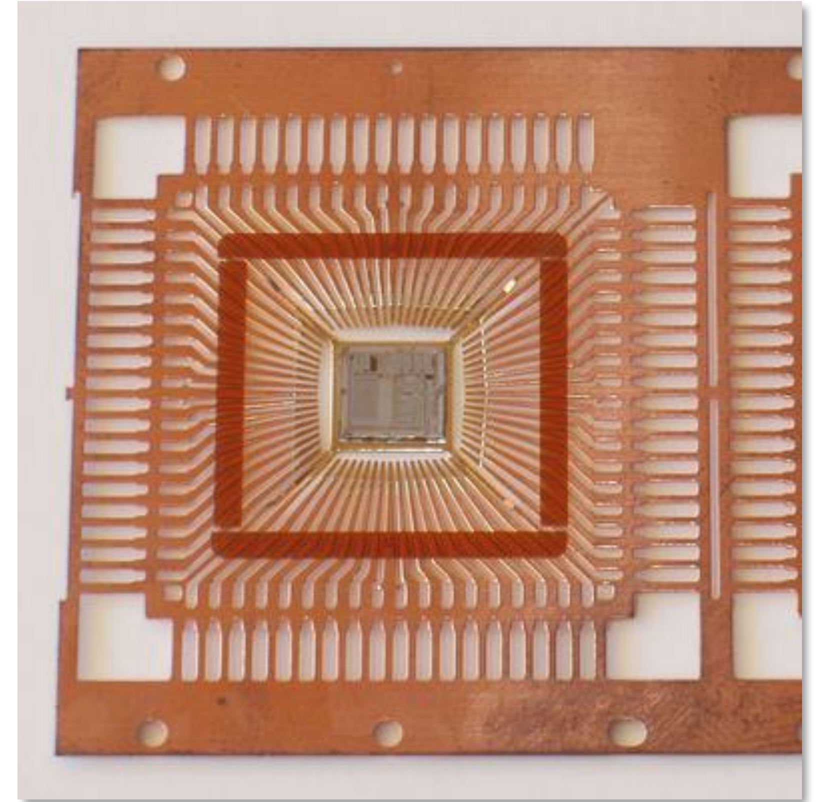
Saw Street

- The wafer must be cut to single dice first.
- A “saw street” (a.k.a. cut line) is a **distance between** two dice.
- This distance (~100 µm) can be used for **process monitor** devices
- This area (kerf) is lost when the die is cut.
- Some wafers needs to be thinner
  - It is called “Wafer **backgrinding**”
  - It must be done before the sawing

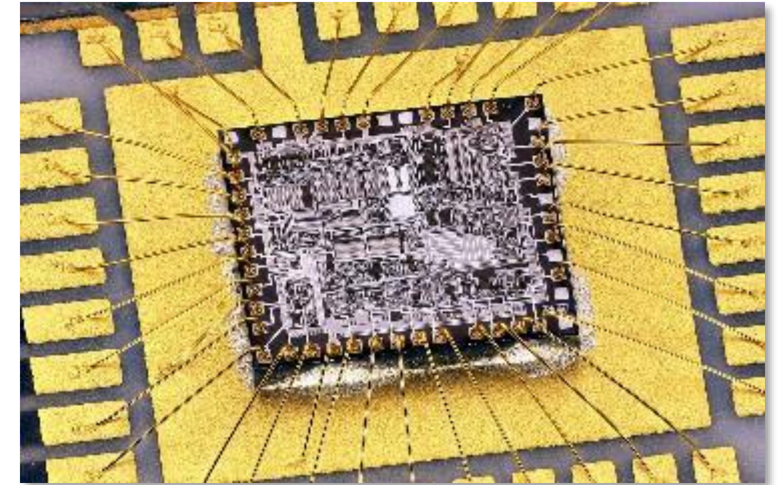


Lead Frame (Not Only) For Leaders

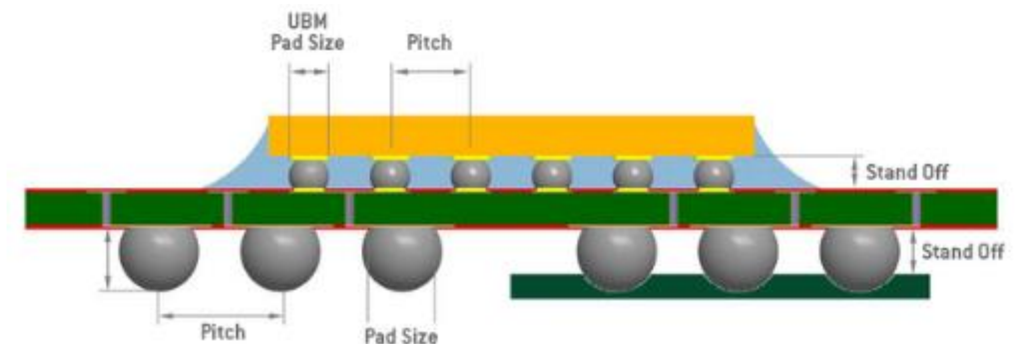
- A **backbone for a package**
  - Holds the die
  - Creates connection paths
  - Defines a package
- Used material (E3, E4) defines the LF properties including the maximal temperature
- The die is glued
- Pads and LF are bonded



Wire Bonding, if Your Chip is not Flipped



- **Wire bonding** is a connection between a bonding pad on the die and the lead frame
  - The wire (Au, Ag , Al, Cu) is very thin (10 – 100 μm)
- **Flip-chip** does not use bonding pads nor wires – there are "bumps"
  - The die is upside down



Many Different Packages to Deliver the Die

- Chip package molding is the final process of a chip manufacturing
- It is the “**small black thing with silver legs**” what is usually called “**a chip**”
- There are tons of different package types and sizes
  - Plastic, ceramic
  - Dual-In-Line, Quad, BGA, PGA, TO-3

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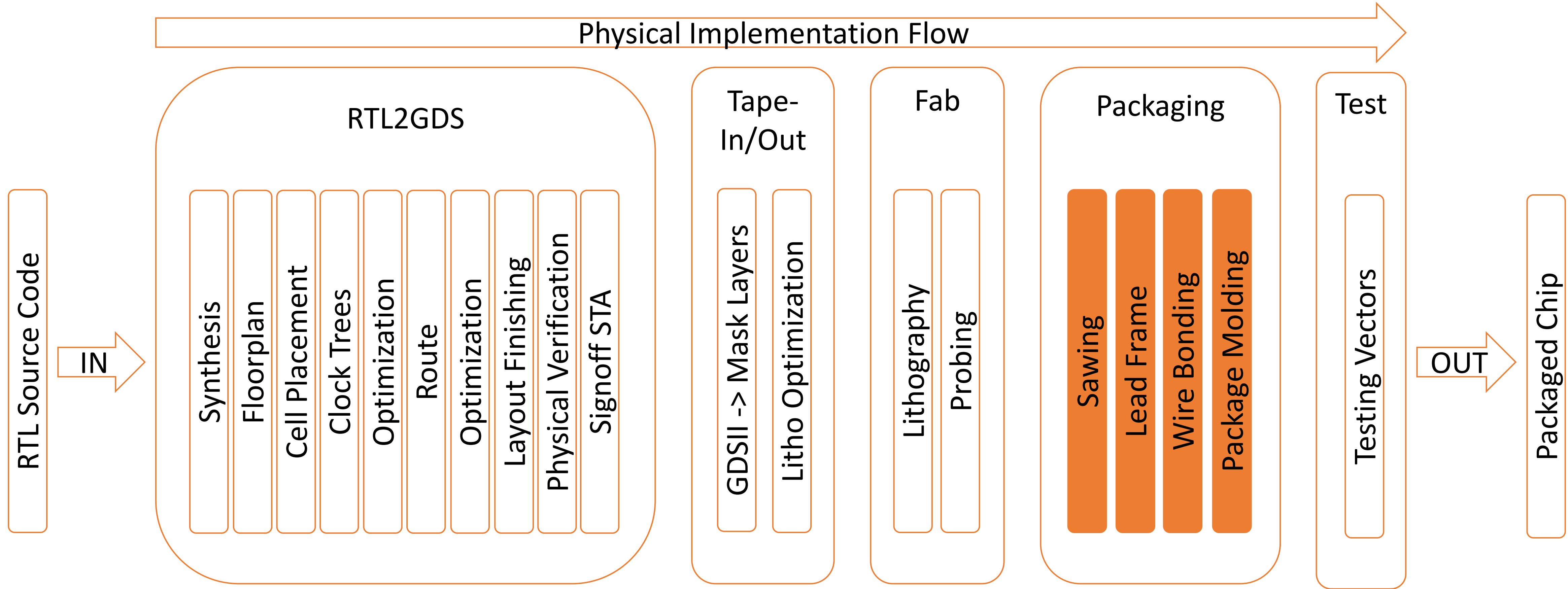
Path from Inputs to Outputs



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Test

Make sure that your chip is working

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DFT, Part Two - ATPG

- All production chips must be tested to prove they are OK
- **A**utomatic **T**est **P**attern **G**eneration is a method to find an input sequence which causes an error or a failure
  - Input patterns (**vectors**) are generated by a tool based on the design (Verilog)
  - Different fault models can be used (e.g. “stuck-at”, bridging, …)
  - Scan-chain design (DFT) is the most common used method

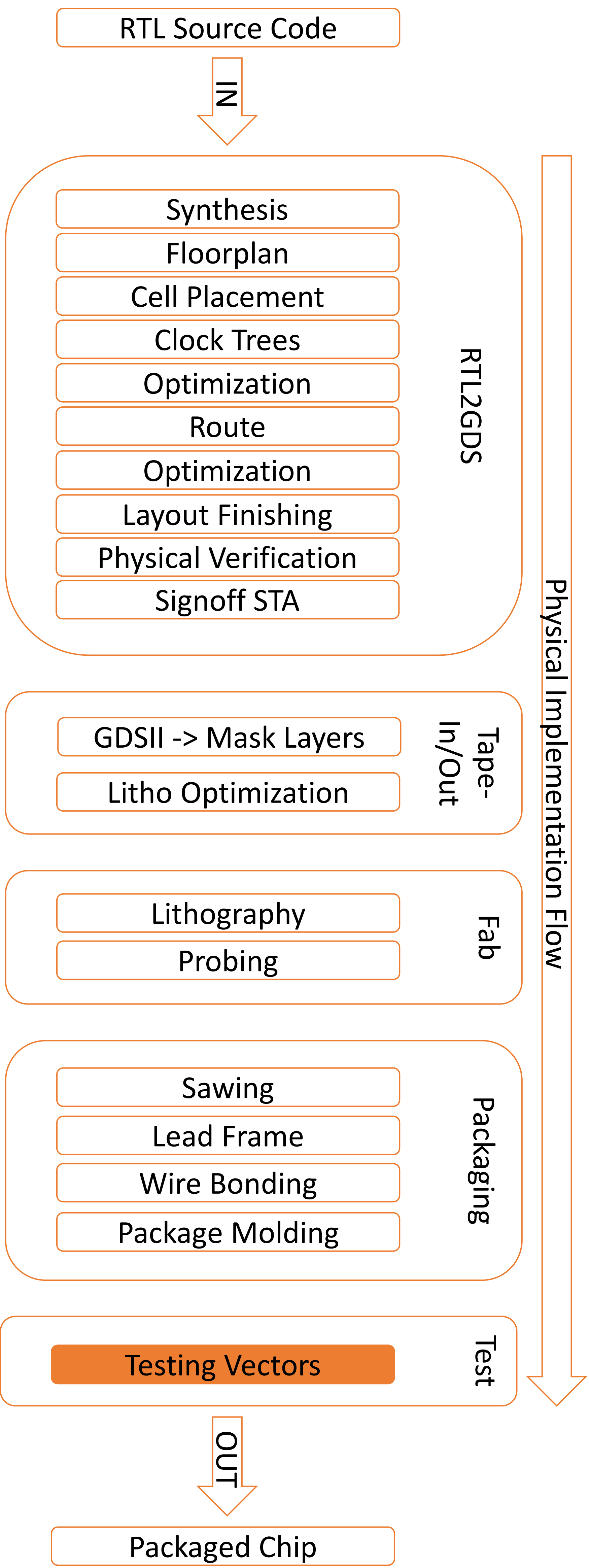
Time is Money. Especially in Testing.

- Each chip is tested and it takes some time.
  - Total time needed for testing is:

$$T_{total} = N * \left(\overline{T_{\text{handling}}} + T_{\text{test1}} + T_{\text{test2}} + T_{\text{test}X}\right), where\ N\ is\ number\ of\ chips$$

- **Important**: If you **reduce testing time** by one second, you can save 11 and half days to test one million chips.
  - It save a huge amount of money.

Path from Inputs to Outputs



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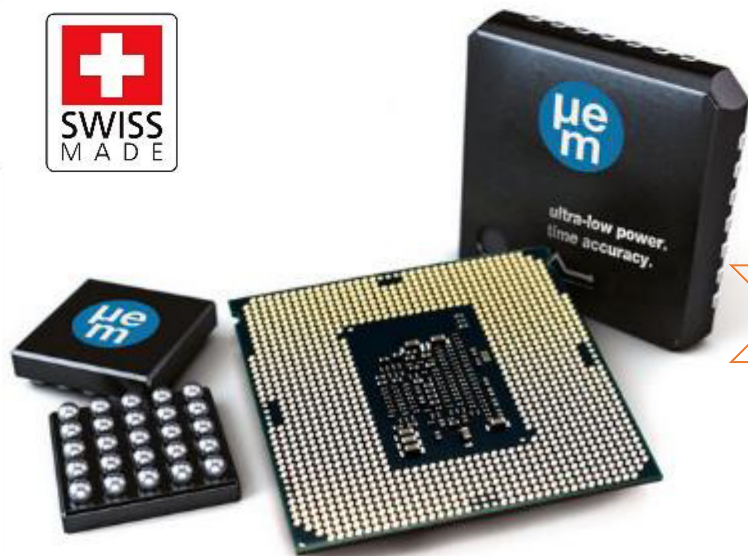
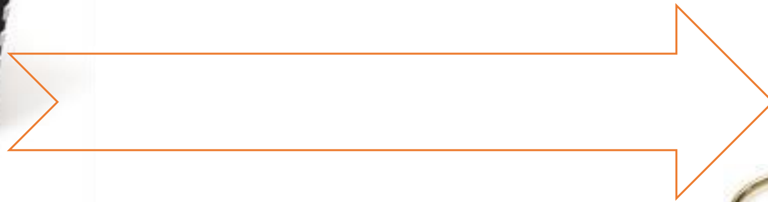
Final Part

Products

Your Chips are Done. Now You Have to Sell Them.





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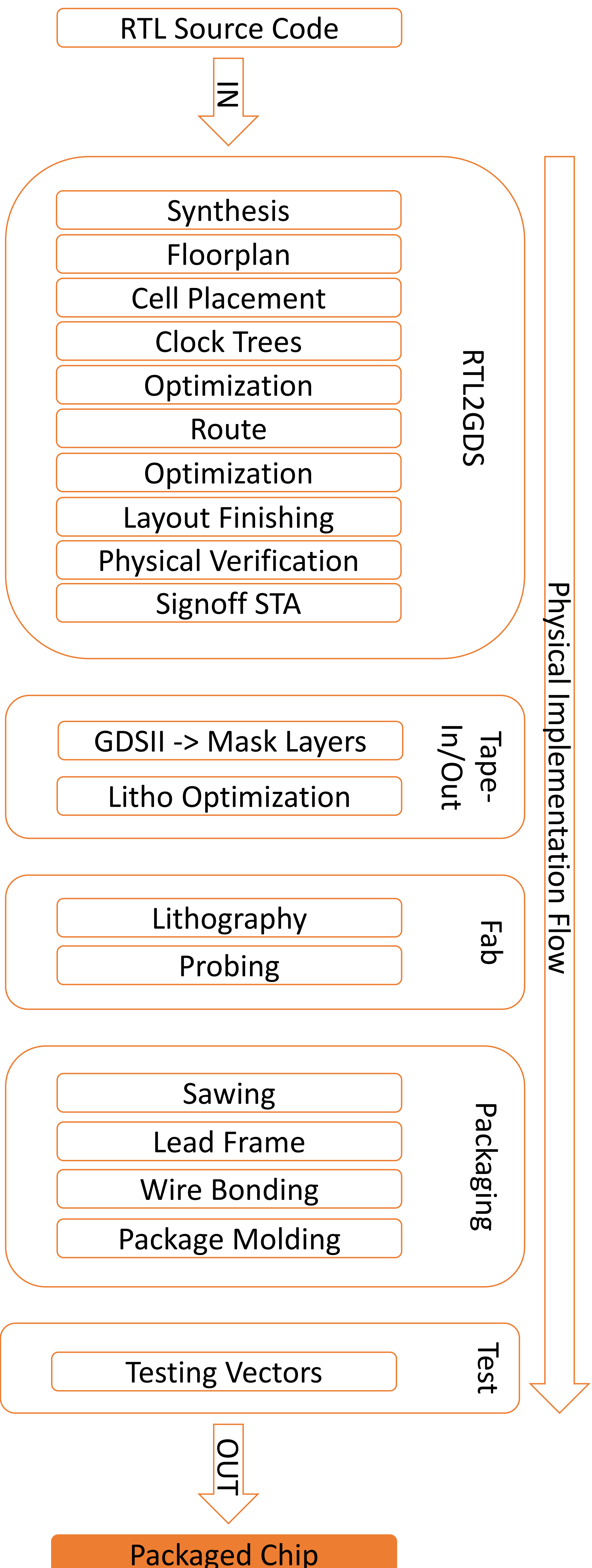

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Thank You For Your Attention

HLEDÁ SE KOLEGA

HOMO TECHNICUS!

Koho hledáme

- Digital Designer
- Digital Verification Engineer
- Embedded Software Engineer
- Validation Engineer
- Backend Engineer

Co nabízíme

- Naučíte se navrhovat integrované obvody
- Praktické zkušenosti z projektů
- Být součástí týmu
- Studentské projekty
- Diplomové práce
- Pracovní doba přizpůsobená Vašemu rozvrhu

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Other

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